What is claimed is:

1. A method executed in a processor comprising:

receiving a request to perform an enqueue or a dequeue operation with respect to a particular queue; and

referencing a corresponding queue descriptor stored in a cache in a processor's memory controller logic to execute the operations, the queue descriptor specifying a structure of the queue.

2. The method of claim 1 further comprising:

maintaining a list of addresses of a subset of queue descriptors stored in a memory in a content addressable memory.

3. The method of claim 2 further comprising:

storing in the cache a queue descriptor corresponding to each address in the list.

4. The method of claim 3 further comprising:

tracking an address stored in the content addressable memory, the address corresponding to a queue descriptor that was least recently used for an enqueue or dequeue operation.

5. The method of claim 4 further comprising:

removing the least-recently-used address from the list if the list lacks an entry corresponding to the queue specified by the request; and

replacing the removed address with an address corresponding to the specified queue.

6. The method of claim 3 further comprising:

issuing commands to the memory controller logic to return and fetch queue descriptors to and from the memory to maintain coherence between the queue descriptors in the cache and the list of addresses in the content addressable memory.

7. The method of claim 6 further comprising:

modifying the queue descriptor referenced by the enqueue or dequeue operation; and

returning the modified queue descriptors to memory from the cache.

8. The method of claim 1 further comprising:

executing an enqueue operation without waiting for completion of a previous dequeue operation.

9. An apparatus comprising:

a memory to store queue descriptors, each of which specifies a structure of a respective queue;

a network processor coupled to the memory further comprising:

memory controller logic that includes a cache to store a subset of the queue descriptors in the memory; and

a programming engine that accesses a list of addresses in the memory corresponding to the queue descriptors stored in the cache; and

wherein the processor is configured to reference a corresponding queue descriptor in the cache in response to a request to perform an enqueue or a dequeue operation with respect to a particular queue.

10. The apparatus of claim 9 wherein the programming engine includes a content addressable memory to store the list of addresses.

11. The apparatus of claim 10 wherein the content addressable memory is configured to track which address in the list was least recently used by the processor for an enqueue or dequeue operation.

12. The apparatus of claim 9 wherein the programming engine is configured to:

remove the least-recently-used address from its list of addresses if the list lacks an entry corresponding to the queue specified by the request; and

replace the removed address with an address corresponding to the specified queue.

13. The apparatus of claim 9 wherein the programming engine is configured to issue commands to the memory controller logic to return and fetch queue descriptors to and from memory to maintain coherence between the queue descriptors in the cache and the list of addresses in the programming engine.

14. The apparatus of claim 9 wherein the processor is configured to return to memory from the cache a queue descriptor modified by an enqueue or dequeue operation.

15. The apparatus of claim 9 wherein the processor is configured to execute an enqueue operation without waiting for completion of a previous dequeue operation if the queue would otherwise be unempty upon completion of the dequeue operation.

16. An article comprising a computer-readable medium that stores computer-executable instructions for causing a computer system to:

reference a queue descriptor stored in a cache in a processor's memory controller logic, in response to receiving a request to perform an enqueue or dequeue operation with respect to a particular queue, the queue descriptor specifying the structure of the queue

17. The article of claim 16 comprising instructions for causing the computer system to:

maintain in a content addressable memory a list of addresses of a subset of queue descriptors stored in a memory.

18. The article of claim 17 comprising instructions for causing the computer system to:

store in the cache a queue descriptor corresponding to each address in the list.

19. The article of claim 18 comprising instructions for causing the computer system to:

track an address in the content addressable memory, the address corresponding to a queue descriptor that was least recently used for an enqueue or dequeue operation.

20. The article of claim 19 comprising instructions for causing the computer system to:

remove the least-recently-used address from the list if the list lacks an entry corresponding to the queue specified by the request; and

replace the removed address with an address corresponding to the specified queue.

21. The article of claim 18 comprising instructions for causing the computer system to:

issue commands to the memory controller logic to return and fetch queue descriptors to and from the memory to maintain coherence between the queue descriptors in the cache and the list of addresses in the content addressable memory.

22. The article of claim 21 comprising instructions for causing the computer system to:

return a queue descriptor modified by an enqueue or dequeue operation from the cache to memory.

23. The article of claim 16 comprising instructions for causing a computer system to:

execute an enqueue operation without waiting for completion of a previous dequeue operation if the queue would otherwise be unempty upon completion of the dequeue operation.